Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**.120”**

**.120”**

**ANODE**

**.112 x .112”**

**Top Material: CrAgAu**

**Backside Material: CrAgAu**

**Bond Pad Size = .112 x .112**

**Backside Potential: CATHODE**

**APPROVED BY: DK DIE SIZE .120” X .120” DATE: 9/2/21**

**MFG: MICROSEMI THICKNESS .012” P/N: 1N5629A**

**DG 10.1.2**

#### Rev B, 7/1